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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,020	06/24/2003	Frederic Reblewski	003921.00135	7641

22907 7590 10/05/2007

BANNER & WITCOFF, LTD.
1100 13th STREET, N.W.
SUITE 1200
WASHINGTON, DC 20005-4051

EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	
MAIL DATE	**DELIVERY MODE**
10/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/602,020	REBLEWSKI ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10 and 16-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-10 and 16-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-2, 8-10 and 16-32 has/have been presented for examination based on amendment filed on 29th August 2007.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 29th August 2007 has been entered.
3. Claim(s) 1, 10, 17, 20 and 23 is/are amended.
4. Claim(s) 3-7 and 11-15 is/are cancelled.
5. Claim(s) 32 is/are new claim(s) added with this amendment.
6. Claim(s) 1-2, 8-10 and 16-32 remain rejected under 35 USC § 103.
7. The arguments submitted by the applicant have been fully considered. Claims 1-2, 8-10 and 16-32 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

8. Examiner withdraws the claim rejection(s) under 35 USC § 103 to claim(s) 1-31 in view of the applicant's amendment.

9. Examiner withdraws the claim rejection(s) under 35 USC § 112 to claim(s) 1 in view of the applicant's amendment.

Specification

10. Claim 32 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 32 discloses limitation such that second sample is stored as to be contiguous with the first sample. However this does not address the situation where the first buffer is full and can no longer hold the second data as indicated by claim 1. Hence the claim 32 contradicts limitations presented in the claim 1.

Response to Remarks regarding Claim Rejections - 35 USC § 103

11. Regarding Claim 1 & 20

New grounds of rejection are presented for these claims therefore the remarks are considered to be moot.

12. Regarding Claim 29

Although new grounds of rejection are presented for this claim, same reference (Litt) is used to reject the argued limitation. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the

features upon which applicant relies (i.e., fill rate associated to particular source) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

As for argument:

> Office Action, p. 4. Respectfully, however, Litt does not teach this at all. In Litt, there is not a smart buffer for each trace chain. Instead, a front-end multiplexer 215 interfaces between the plurality of sources and the smart buffers, sending data to various smart buffers as appropriate. While it is true that arbitration logic 250 can detect whether a smart buffer is "under pressure," this pressure is not related to the data fill rate of any particular source. Again, that is because a given smart buffer is not associated with a given source. Rather, the smart buffers are a shared resource because of the intervening front-end multiplexer 215.
>
> Thus, in Litt, arbitration logic 250 is completely isolated from knowing about the data fill rates of given sources. There is simply no teaching of selecting smart buffers based on any property at all of the sources; arbitration logic 250 is aware only of the smart buffers themselves. Respectfully, the proposed modification has no basis in Litt. Nor does the proposed modification have a basis in Swoboda. Swoboda mentions dynamic pin assignment but says little more about the subject, and certainly does not discuss how such dynamic pin assignment would operate.

Examiner respectfully disagrees as fill rate is obviously the basis of the pressure exerted on the buffer. Litt states:

Litt: Col.12 Lines 3-31:

> The arbitration may be configured with various arbitration protocols to insure that the smart buffers 225a, 225b are permitted to *unload their data in timely fashion so as not to lose important data that is being presented at the upstream end*.
>
> According to the preferred implementation for the arbitration logic, the arbitration logic 250 is configured to accept data from a particular buffer if that is the only channel of interest to the user. Preferably, each stream is treated as being of equal importance, and the arbitration rules apply equally to both streams. If both channels have been selected for off-loading by the user, then the arbitration logic 250 must examine the control bits that indicate if the buffer slot is full and the relative importance of the tick in that memory slot. Thus, the arbitration logic 250 determines which buffer 225a, 225b to accept data from based on the status of the important and full bits associated with the data in the downstream slot of each buffer. In addition, the arbitration logic 250 may also receive a signal indicating if a buffer is not under pressure because one or more empty slots exist in the buffer. *This can be implemented in a variety of ways, including, for example, determining if a particular slot (such as the back slot) is empty, or if any other slots in the buffer are empty (by ORing together the empty bits from the smart buffer), or by receiving the empty signal bit from all or a subset of all of the memory slots.* Regardless of the specific implementation, the arbitration logic 250 preferably is capable of detecting if any slots in a buffer are empty so that it can determine if the buffer is under pressure.

According to the exemplary embodiment, the arbitration logic 250 will select data from a smart buffer if that buffer is under pressure but the other buffer is not. Thus, regardless of the data in the downstream slot of the buffers, the arbitration logic will select data from the buffer, which is under pressure. If both buffers are under pressure or if neither buffer is under pressure, then the arbitration logic will select the buffer, which has the more important data. If both buffers are of equal pressure and the data in the downstream slot if of equal importance, then the arbitration logic 250 implements a round-robin approach where it will alternatively select the downstream slot from each buffer.

Referring still to FIG. 2, the clock circuit 275 preferably receives a clock mode signal, which may be user programmable. The clock mode signal preferably designates the clock speed at which data is to be output from the output port 150. *According to the preferred embodiment, in response to the status of the clock mode signal, the clock circuit 275 either selects a predetermined output rate, or else selects a clock rate that is determined based on the selected data source.* If the clock circuit 275 uses the clock of the data source, the clock circuit 275 preferably divides the forwarded clock by an appropriate divisor based on the selected source data and number of enabled smart buffers to obtain a suitable output clock.

As for Swoboda, the current Litt & Swoboda reference teaches pin manager with various output pin configuration based on the input clock rate of the source. See Swoboda: Fig.23, 23A-B; Litt: besides what disclosed above Col.12 Line 56-Col.13 Line28. Examiner finds applicant's arguments unpersuasive and presents the updated rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 1-2, 8-10 and 16-32 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0065642 A1 by Gary L. Swoboda (Swoboda hereafter), in view of U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter), further in view of US Patent No. 6092127 issued to Eric G. Tausheck (Tausheck hereafter).

Regarding Claim 1

Swoboda teaches a method in an emulation system (Swoboda: Fig.2 & associated disclosure), comprising receiving a first sample of state data (Swoboda: Fig.9 & and associated disclosure); selecting data of interest from the first sample, wherein the data of interest is a subset of bits of first sample and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest (Swoboda: Fig.19 & [0121]).

Further Swoboda teaches storing the data for transmission such that first and second portions of the data of interest are no longer separated by at least a bit as selecting the data of interest from the packet (Swoboda: Fig.19 & [0121]) and then aligning them for transmission (Swoboda: [0122]-[0128], [0130] & Fig.2, 8, 21, 22 and 23, 23 A-B).

Although Swoboda is concerned with storage of trace information, through compression (Swoboda: [0117]-[0118]) it does not explicitly teach determining residual storage of trace buffer and selecting the next buffer if the first buffer is full.

Litt teaches determining if residual storage space in a first buffer exists as smart buffers, which are aware of the buffer state (full or available) of each location in the

smart buffer (Litt: Col.10 Lines 12-46). Litt also teaches receiving a first sample of state data (Litt: Col.8 Lines 33-48), sorting the first sample (Litt: Col.7 Lines 20-67), and storing the sorted first sample in the smart buffer (Litt: Fig.2).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Litt to Swoboda as Litt & Swoboda are primary concerned with offloading the trace information. The motivation to combine would be that Litt provides arbitration logic to unload multiple trace buffer (Litt: Fig.2 & associated text) lacking in Swoboda to ease the unloading pressure making the system run faster with appropriate prioritization, especially when trace offloading rates are different from trace generation rate (Swoboda: Fig.22, [0128]-[0129]).

Litt in Swoboda do not explicitly teach switching to the second buffer if the first buffer is full for storing the trace information.

Tausheck teaches checking if residual space in the first buffer exists, storing the data in it and if the first buffer is full then storing the data in second buffer (Tausheck: Col.2 Lines 38-45).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Tausheck to Litt & Swoboda as Litt & Swoboda are primary concerned with offloading the trace information, however do not disclose handling of multiple offload buffers. The motivation to combine would be that Litt and Swoboda disclose buffer which are FIFO buffer (Litt: Col.10 Lines 13-37; Swoboda: [0128]), however buffer switching is

not disclosed by either to ease buffer pressure and overflow condition, which is taught by Tausheck as handing multiple DMA buffers is an analogous situation where switching happens between the full buffers (Tausheck: Abstract).

Regarding Claim 2

Litt teaches the step of determining whether the first buffer is full and storing the sorted first sample in the first buffer (Litt: Col.10 Lines 17-46).

Regarding Claim 8

The limitations presented are repetition of the steps performed above in claim 1. They are rejected for the same reasons as claim 1.

Regarding Claim 9

Litt & Tausheck teach smart buffers that decide based on the residual space left in the buffer whether to store the data (Litt: Col.10 Lines 47-60; Tausheck: Fig.3). Swoboda also teaches storing partial information in the buffer (Swoboda: Fig.19).

Regarding Claim 10

Swoboda teaches receiving comprises receiving the first sample of state data from reconfigurable emulation resource (Swoboda: Fig.2-4 [0007][0066]).

Regarding Claim 16

Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 17

Litt teaches storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60).

Regarding Claim 18

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]).

Regarding Claim 19

Claim 19 repeats the limitations of claims 1 & 16, where the subsequent packets are stored in the memory and is rejected for the same reasons as parent claims.Also see Swoboda Fig.22 and 22A.

Regarding Claim 20

Litt teaches an apparatus having a first select logic device configured to receive samples of state data, to sort samples of state data, and to select data of interest from each of the samples of state data (Litt: Fig.2, Elements 210 & 215, Col.6 Lines 3-34); first and second buffers coupled to the first select logic device and configured to receive the selected data of interest (Litt: Fig.2 Elements 225a 225b); a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer (Litt: Fig.2 Elements 250); and an output storage device coupled to the second select

logic device and configured to receive data drained from the selected buffer (Litt: Fig.1 Element 50).

Litt does not teach select data of interest being filled in an alternating manner in each buffer.

Tausheck teaches that trace data is filled in the alternating manner in the trace buffers and then emptied in the alternating manner (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 21

Litt teaches first select logic comprises a multiplexer (Litt: Fig.2 Elements 245a & 245b).

Regarding Claim 22

Litt teaches second select logic (as arbitration logic) comprises a multiplexer (Litt: Fig.2 Elements 250; Col.11 Line 56-Col.12 Line 43) where the selection between the buffers to offload the data of interest from them.

Regarding Claim 23

Litt & Tausheck teach first select logic device (Litt: 245a & b) is configured to send data if interest to second buffer responsive to first buffer becoming full (Tausheck: Col.5 Lines 62-Col.6 Lines 67 at least).

Regarding Claim 24

Litt teaches the first select logic device comprises a data of interest sorter (Litt: Fig.2 Packet Prediction and parsing logic with the Prioritization of packets; Col.10 Lines 47-Col.11 Line 6).

Regarding Claim 25

Claim 25 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16. Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 26

Claim 26 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17. Litt teaches storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60).

Regarding Claim 27

Claim 27 discloses similar limitations as claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 28

Litt teaches output storage device is configured to store information associated with each of the samples of state data as header to each sample that contains sample relevant data (Litt: Col.6 Line 61- Col.7 Line 19).

Regarding Claim 29

Litt teaches determining a trace data fill rate of each of a plurality of trace data chains as various trace streams with various rates in the bandwidth manager section (Litt: Col.4 Lines 21-25, 55-65); determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data

chains based at least upon the determined trace data chain fill rates as decision to offload data by the arbitration manager based on the pressure on the trace buffer once it gets full due to higher fill rate (Litt: Col.12 Lines 8-31).

Litt does not teach a pin manager explicitly that would perform the steps of offloading the data.

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.22; [0128]).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda to Litt to enhances the Litt's teaching by adding a Pin Manager/macro function to arbitration logic and output section of Litt's teaching. To clarify further, The motivation to combine would have been that Swoboda and Litt are concerned with trace data capture where Swoboda and Litt output the trace data to a debugger (Litt: Fig.2; Swoboda: Fig.2, 22, 23, 23A-B) where the pin management is obvious for such data offloading. Swoboda explicitly discloses the pin manager, where the pins for trace & debug can be dynamically allocated reducing the limited pin count pressure in offloading trace information (Swoboda: Fig.22; [0128]).

Regarding Claim 30

Claim 30 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29. The bandwidth allotment is determined by the arbitration logic and directions from source clock (Litt: Col.12 Lines 57-Col.13 Line 27). Litt does not explicitly teach the pin schedule selection, which is taught by Swoboda (Swoboda:

Col.10 Lines 3-4). Motivation to combine Litt and Swoboda is the same as claim 29 above.

Regarding Claim 31

Claim 31 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30. Litt teaches the limitation where the trace chain data fill rates are determined and matched with the data output rate from the arbitration logic. Arbitration logic multiplexer selects the input (pins) from smart buffer based on the fill rate and distress (due to higher fill rate in a smart buffer) (Litt: Col.11 Lines 56-Col.13 Line 37. Motivation to combine Litt and Swoboda is the same as claim 29 above.

Regarding Claim 32

Swoboda teaches a second packet handling similar to the first packet handling (Swoboda: Fig.19, 22A, Fig.23, 23A-B)

Conclusion

14. All claims are rejected.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

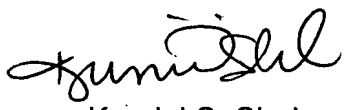
Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Monday, September 24, 2007



Kamini S. Shah
Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation